

1. A method to display a source image on a LCD panel without scaling

comprising the steps of:

transferring an even image line to line buffers,

transferring the output of said line buffers to an input of LCD panel

5 drivers of an upper half portion within the LCD panel.

skipping an LCD Vsync-pl at the end of a display within said even
image lines.

transferring odd image lines to line buffers,

transferring the output of said line buffers to the input of the LCD

10 panel drivers of a lower half portion within the LCD panel,

blanking the data of said odd image of said lower portion of the
LCD screen.

2. The method of displaying a source image on an LCD panel without scaling of

15 claim 1 further comprising the steps of:

moving a no-scaling image up or down on the LCD panel by
shifting the timing of the vertical synchronization Vsync of the LCD panel to the
left or right in the time domain.

20 3. The method of displaying a source image on an LCD panel without scaling of

claim 1 further comprising the steps of:

limiting the requirement for a frame buffer.

4. A method of displaying a source image on an LCD panel without scaling and without an image buffer comprising the steps of:

skipping on vertical synchronization pulse every two normal vertical sync time periods,

- 5 displaying the even lines of the source image,
blanking the lower portion of the LCD image and,
shifting the vertical synchronization pulse in order to shift the LCD image to the center of the LCD displayable area.

- 10 5. An apparatus to display a source image on a LCD panel without scaling comprising:

a means for transferring an even image line to line buffers,

a means for transferring an output of said line buffers to an input of LCD panel drivers of an upper half portion within the LCD panel.

- 15 a means for skipping LCD Vsync-pl at the end of a display within said even image lines,

a means for transferring odd image lines to line buffers,

a means for transferring an output of said line buffers to an input of LCD panel drivers of a lower half portion within the LCD panel.

- 20 a means for blanking data of said odd image of said lower portion of the LCD screen.

6. The apparatus of claim 5 further comprising:

a means for moving a no-scaling image up or down on the LCD panel by shifting the timing of the vertical synchronization Vsync of the LCD panel to the left or right in the time domain.

5 7. The apparatus of claim 5 wherein there is no requirement for a frame buffer.

8. The apparatus of claim 5 wherein said means for transferring the even image lines to line buffers further comprising:

10 a means for performing said transfer utilizing direct connections between the output of the image buffer and the line buffers of the LCD panel.

9. The apparatus of claim 5 where said means for transferring the odd image lines to line buffers further comprising:

15 a means for performing said transfer utilizing direct connections between the output of the image buffer and the line buffers of the LCD panel.

10. The apparatus of claim 5 where said means for transferring the output of said line buffers to the input of the LCD panel drivers of the upper half portion within the LCD panel further comprising:

20 a means for performing said transfer utilizing direct connections between said line buffers and said LCD panel drivers.

11. The apparatus of claim 5 where said means for skipping the LCD Vsync-pl
at the end of a display within said even image lines further comprising:

a means for performing said skipping utilizing a frequency divider to
divide the image source buffer Vsync by two.

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12. The apparatus of claim 5 where said means for blanking the data of said odd
image of said lower portion of the LCD screen further comprising:

a means for performing said blanking utilizing a logic circuitry which
senses the odd frame time domain.

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13. The apparatus of claim 6 where said means for moving the no-scaling image
up or down on the LCD panel by shifting the timing of the vertical
synchronization signal, Vsync of the LCD panel to the left or right in the time
domain further comprising:

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a means for performing said moving of Vsync for the LCD panel by
utilizing a shift register to shift the Vsync the required amount to the left or right in
the time domain.

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14. An apparatus for displaying a source image on an LCD panel without scaling
and without an image buffer comprising:

a means for skipping on vertical synchronization pulse every two
normal vertical sync time periods,

a means for displaying the even lines of the source image,

a means for blanking the lower portion of the LCD image and,

a means for shifting the vertical synchronization pulse in order to shift the LCD image to the center of the LCD displayable area.

- 5 15. A program retention device containing program instruction code executable on at least one networked computing device for simulating a model of an LCD panel without scaling, whereby said program performs the steps of:

transferring the even image line to line buffers,

transferring the output of said line buffers to the input of the LCD

- 10 panel drivers of the upper half portion within the LCD panel.

skipping the LCD Vsync-pl at the end of a display within said even image lines.

transferring the odd image lines to line buffers,

transferring the output of said line buffers to the input of the LCD

- 15 panel drivers of the lower half portion within the LCD panel.

blanking the data of said odd image of said lower portion of the LCD screen.

16. The program retention device of claim 15, wherein said program further
20 performs the step of:

moving the no-scaling image up or down on the LCD panel by

shifting the timing of the vertical synchronization Vsync of the LCD panel to the left or right in the time domain.

17. The program retention device of claim 15, wherein said program eliminates the requirement for a frame buffer.

5 18. A program retention device for displaying a source image on an LCD panel without scaling and without an image buffer, whereby said program performs the steps of:

skipping on vertical synchronization pulse every two normal vertical sync time periods,

10 displaying the even lines of the source image,

blanking the lower portion of the LCD image and,

shifting the vertical synchronization pulse in order to shift the LCD image to the center of the LCD displayable area.

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